REMARKS

In the Official Action mailed 11 January 2007, the Examiner withdrew the double patenting rejection; rejected claims 1 and 15 under 35 U.S.C. §112; rejected claims 1-2, 4-6, 8 and 14-15 under 35 U.S.C. §102(e); and rejected claims 3, 7 and 9-13 under 35 U.S.C. §103(a).

Claims 1-15 remain pending and new claims 18-19 have been added. Applicant respectively traverses the rejections below.

Rejection of Claims 1 and 15 under 35 U.S.C. §112

The Examiner has rejected claims 1 and 15 under 35 U.S.C. §112, paragraph 2, for indefiniteness in that the limitation "the configuration memory" recited in claim 1, lines 6-7 and claim 15, line 4 lack antecedent basis.

Applicant has amended claims 1 and 15 to correct the specific antecedent concerns raised by the Examiner in the Office Action. Specifically, Applicant has added "programmable" to be consistent in the claim language. Applicant has also similarly amended claim 14. Applicant submits that claims 1 and 15 as amended are in a condition for allowance.

Accordingly, reconsideration of the rejection of claims 1 and 15 is respectfully requested.

Rejection of Claims 1-2, 4-6, 8 and 14-15 under 35 U.S.C. §102(e)

The Examiner has rejected claims 1-2, 4-6, 8 and 14-15 under 35 U.S.C. §102(e) as being anticipated by Ikeda et al. (US 2003/0184339), hereinafter referred to as "Ikeda". Applicant respectfully requests reconsideration.

For at least the reasons stated below, Applicant asserts that Ikeda fails to expressly or inherently describe each and every element of the invention claimed by the applicant.

Independent claim 1 has been amended from "a programmable configuration memory" to include "a programmable non-volatile configuration memory". Claims 8-10 and 14-15 have been amended to be consistent in the claim language. This amendment to claim 1 contains no new matter and adds the limitation of "non-volatile" which was previously included in dependent claim 11, which has now been canceled.

In the rejection of claim 1, the Examiner states that Ikeda teaches "a configurable logic array (i.e. the Offchip FPGA 14 in Fig. 1) having a programmable configuration defined by

configuration data stored in electrically programmable configuration points within the configurable logic array..." (Office Action, page 3).

Applicant respectfully submits that it is incorrect to read the configurable logic array of claim 1 on the "Offchip FPGA" of Ikeda. Further, as explained below, Applicant submits that Ikeda does not disclose "a programmable non-volatile configuration memory" as required by amended claim 1 of the present invention.

Ikeda does not disclose the manner in which the Offchip FPGA is programmed. Thus, Ikeda does not disclose a configuration function associated with the FPGA. Ikeda only discloses that the FPGA supports a programmable matrix (Ikeda, Figure 1, ref. no. 20) in the processing of data. See, Ikeda, Figures 1 and 11(a), and paragraphs [0052] and [0077]. Additionally, Ikeda discloses that an advantage of his invention of programming a matrix instead of programming the FPGA is "[w]ith this integrated circuit device, there is no need to change all the connections at the transistor level as is the case with an FPGA, so that the hardware can be reconfigured in a short time." (Ikeda, paragraph [0005]).

One could take the position that the programmable logic array of claim 1 of the present invention reads on the matrix disclosed by Ikeda. Ikeda does describe configuring the matrix. However, even if one takes the position that the programmable logic array of claim 1 reads on the matrix disclosed by Ikeda, Applicant submits that claim 1 of the present invention is patentably distinct from Ikeda because Ikeda does not disclose "a programmable non-volatile configuration memory" as required by amended claim 1 of the present invention.

Regarding the amendment of claim 1 made herein to include the limitation "non-volatile" which was previously included in claim 11, the Examiner states in the 35 USC 103(a) rejection of claims 11-13 that "Ikeda teaches that the programmable configuration memory comprise floating gate memory cells, i.e. charge programmable memory cells (i.e. the FPGA10 in Fig. 17). However, Ikeda does not clarify whether these cells are non-volatile or not." (Office Action, page 8).

In the above cited comment by the Examiner, it is unclear what "cells" of Ikeda the Examiner is referencing with "the FPGA10 in Fig. 17" or how the programmable configuration memory of the present invention reads on it. Ikeda does not disclose an FPGA with a reference number 10, and Figure 17 of Ikeda "shows an example of an intermediate language description" (Ikeda, paragraph [0046]) and appears to be completely unrelated to any type of memory cells.

Further, in a search of Ikeda no reference to "floating gate memory cells" or "charge programmable memory cells" were found.

In the rejection of claims 11-13 the Examiner further states "it is well-known and notorious old in the art at the time the current invention was made to combine both the volatile and nonvolatile cells in the FPGA memory." (Office Action, page 8). Applicant respectfully submits that the Examiner's motivation to modify in the above cited comment does not appear to be related to claims 11-13 in the present application. Claim 11 relates to programmable non-volatile configuration memory, claim 12 relates to programmable volatile configuration memory, and claim 13 relates to non-volatile charge programmable memory cells. None of the claims recite a combination of both volatile and nonvolatile memory or relate to an "FPGA memory".

One could argue that the configuration memory of amended claim 1 reads on the processor memory disclosed by Ikeda. Ikeda discloses in paragraph [0052] that the processor 11 can be constructed with internal memory (RAM or ROM) and that the execution program 3 can be stored in the processor memory. Because Ikeda discloses that the processor memory is either RAM or ROM, Ikeda does not disclose the processor memory comprising programmable non-volatile memory. Additionally, Ikeda seems to imply that RAM is used for the processor memory because Ikeda discloses that a new execution program must be compiled and loaded into processor memory every time the operation units of the matrix needs to be reconfigured. See, Ikeda, paragraphs [0100]-[0104].

Many problems not addressed by Ikeda's invention are solved by the present invention having a programmable non-volatile configuration memory. One problem solved by the present invention is that the configurable logic array can be implemented by a standard FPGA having volatile configuration points and the configuration data will remain stored on the integrated circuit when power is removed from the system. Other problems solved include that the configuration function may be simplified, and that the configuration data can be stored in an encrypted and/or compressed format as recited in dependent claims 9 and 10.

Therefore, for at least the reason that Ikeda does not disclose "a programmable non-volatile configuration memory", claim 1 is patentably distinct from Ikeda.

Claims 2, 4-6, 8 and 14-15 depend from claim 1, and are patentable for at least the same reasons as claim 1. Accordingly, reconsideration of the rejection of claims 1, 2, 4-6, 8 and 14-15 as amended are respectfully requested.

Rejection of Claim 3 under 35 U.S.C. §103(a)

The Examiner has rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Hsu et al. (US 5359570).

Claim 3 depends from claim 1 and neither Ikeda, as discussed above, nor Hsu et al. disclose the elements of claim 1 as amended. Therefore claim 3 is patentable for at least the reasons discussed above and because of the unique combinations recited. Accordingly, reconsideration of the rejection of claim 3 is respectfully requested.

Rejection of Claim 7 under 35 U.S.C. §103(a)

The Examiner has rejected claim 7 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Sun et al. (US 6401221).

Claim 7 depends from claim 1 and neither Ikeda, as discussed above, nor Sun et al. disclose the elements of claim 1 as amended. Therefore claim 7 is patentable for at least the reasons discussed above and because of the unique combinations recited. Accordingly, reconsideration of the rejection of claim 7 is respectfully requested.

Rejection of Claim 9 under 35 U.S.C. §103(a)

The Examiner has rejected claim 9 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Sun et al. (US 5901330), hereinafter referred to as "Sun2".

Claim 9 depends from claim 1 and neither Ikeda, as discussed above, nor Sun2 disclose the elements of claim 1 as amended. Therefore claim 9 is patentable for at least the reasons discussed above. Accordingly, reconsideration of the rejection of claim 9 is respectfully requested.

Rejection of Claim 10 under 35 U.S.C. §103(a)

The Examiner has rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Lawman (US 6028445), hereinafter referred to as "Lawman".

Claim 10 depends from claim 1 and neither Ikeda, as discussed above, nor Lawman disclose the elements of claim 1 as amended. Therefore claim 10 is patentable for at least the

reasons discussed above and because of the unique combinations recited. Accordingly, reconsideration of the rejection of claim 10 is respectfully requested.

Rejection of Claims 11-13 under 35 U.S.C. §103(a)

The Examiner has rejected claims 11-13 under 35 U.S.C. §103(a) as being unpatentable over Ikeda.

Claims 11-12 have been canceled. Claim 13 depends from claim 1 and Ikeda, as discussed above, does not disclose the elements of claim 1 as amended. Therefore claim 13 is patentable for at least the reasons discussed above and because of the unique combinations recited. Accordingly, reconsideration of the rejection of claim 13 is respectfully requested.

New Claims 18-19

Applicant has added new dependent claims 18-19. The new claims are fully supported by the specification and drawings as filed and do not add new matter.

Claim 18 finds support in Figure 6 and paragraph [0044]. Claim 19 finds support in Figure 5 and paragraphs [0042]-[0043].

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1522-1).

Respectfully submitted,

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